UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,174	12/11/2003	Masaaki Oka	SCES 20.808 (100809-00230	5945

26304 7590 10/23/2009

KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
ARCOS, CAROLINE H	
ART UNIT	PAPER NUMBER
2195	
MAIL DATE	DELIVERY MODE
10/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,174	OKA ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/02/2009 has been entered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

i. The operating environments- claim 7.

ii. The contents- claim 8.

iii. The application program, the assigned function- claim 10

b. The claim language in the following claims is not clearly understood:

i. As per claim 7, line 13, it is not clearly understood what is meant by "setting the operating environment" (i.e. operating system or mode of operation: serial or parallel).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1).

4. As per claim 1, Branco teaches the invention substantially including a signal processing device, comprising:

a general-purpose signal processor formed of an assembly of plural component-processors (abs., lines 1-10);

a management processor that configures connections for each of the component-processors in accordance with a demand for signal processing (abs., lines 14-16; col. 3, lines 43-67; col. 4, lines 1-12);

wherein the management processor estimates a type of processing and determines based on the estimation a number of component- processors to operate (col. 3, lines 60-67; col. 4, lines 1-12), and

wherein said management processor configures connections of each of the

component-processors(abs., lines 14-16; col. 3, lines 43-67; col. 4, lines 1-12) .

5. Branco does not explicitly teach estimates an entire load and determines based on the estimation a number of component- processors to operate, and loads application programs into the component-processors.

6. However, Rawson teach estimates an entire load and determines based on the estimation a number of component- processors to operate, and loads application programs into the component-processors (abs., lines 1-18; par. [0007]; par. [0017]; par. [0018]; claim 17).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Rawson because Rawson teaching of estimating the workload and determines based on the estimation a number of component- processors to operate would benefit the system performance, improve system resource usage and increase power saving.

8. As per claim 2, Branco teaches an input/ output interface for receiving a signal to be processed inputed from an external device or one of the component-processors (col. 1, lines 45-67; col. 2, lines 1-15; col. 5, lines 37-67) and wherein the management processor controls the input/output interface to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with a demand for signal processing (col. 1,

lines 50-55; col. 3, lines 43-67).

9. As per claim 5, Branco teaches a local memory is disposed on each of the component-processors, said local memory stores a signal to be processed or a signal processed result by the component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface (col. 1, lines 46, lines 49; col. 2, lines 35-38).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1), as applied to claim 2 above and further in view of Macias et al. (US 5,886,537).

11. As per claim 3, the combined teaching of Branco and Rawson does not explicitly teach the input/output interface includes a cross bus switch that can selectively connect, the external device to one of the component-processors, or the component-processors to each other.

12. However, Macias teaches the input/output interface includes a cross bus switch that can selectively connect, under the control of the management processor, the external device to one of the component-processors, or the component-processors to each other (Fig. 1).

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Branco, Rawson and Macias because Macias teaching of a cross bus switch that can connect the component-processors to each other would allow easier communication between different processor in the system.

14. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1) as applied to claim 2 above and further in view of Iwase et al. (US 5,926,583).

15. As per claim 4, the combined teaching of Branco and Rawson doesn't explicitly teach the input/output interface includes a multiple bus that can connect the component-processors to each other.

16. However, Iwase teaches the input/output interface includes a multiple bus that can connect the component-processors to each other (col. 31, lines 18-45).

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson and Iwase because Iwase teaching would regulate communication efficiently between different component of the system.

18. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Rawson, III (US 2003/0115495 A1), as applied to

claim 2 above and further in view of Arnold et al. (US 5,175, 837).

19. Claim 6, the combined teaching of Branco and Rawson does not explicitly teach the general-purpose signal processor, the management processor and the input/output interface are disposed in a single case, the case including a first connection interface being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface.

20. However, Arnold teaches the case including a first connection interface being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface (Fig. 1, element 18, 20A).

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Rawson and Arnold because Arnold teaching would facilitate the communication between different components of the system.

22. The combined teaching does not explicitly teach that the general-purpose signal processor, the management processor and the input/output interface are disposed in a single case. However, it is well known to one of ordinary skill in the art at the time the invention was made to conclude that all three components are disposed on a single case

for portability.

23. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537) and further in view of Rawson, III (US 2003/0115495 A1).

24. As per claim 7, Branco teaches an entertainment device, comprising:

a signal processing device including a general-purpose signal processor (abs., lines 1-13; col. 1, lines 44-67; col. 2, lines 1-67); , a management processor (col. 3, lines 43-67; col. 4, lines 1-12) and an input/output interface (col. 1, lines 50-55; col. 2, lines 39-45); and

wherein said general-purpose signal processor is formed of an assembly of plural component-processors, wherein each of the component-processors operate in parallel independent of other component-processors (abs.; col. 1, lines 37-67; col. 2, lines 1-67);

wherein the management processor sets the operating environments for each of the component-processors in accordance with a demand for signal processing (col. 3, lines 43-67; col. 4, lines 1-12);

the input/output interface so as to swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with the demand for signal processing(col. 1, lines 50-55; col. 2, lines 39-45); and

wherein the management processor estimates a type of processing and determines based on the estimation a number of component-processors to operate, and changes the

operating environment of each of the component-processors (col. 3, lines 43-67; col. 4, lines 1-12).

25. Branco does not explicitly teach a main processor that provides a demand for signal processing to the signal processing device,

wherein the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors, and

wherein the management processor estimates an entire load of processing, and determines based on the estimation a number of component-processors to operate.

26. However Macias teaches the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors (col. 3, lines 31-67; col. 4, lines 1-3; Fig. 1).

27. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Macias because Macias teaching of input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors would be known to one of ordinary skill in the art as one of the function of input/ output interface which facilitate the communication between

different component of the system.

28. The combined teaching of Branco and Macias does not explicitly teach wherein the management processor estimates an entire load of processing, and determines based on the estimation a number of component-processors to operate.

29. However, Rawson teaches the management processor estimates an entire load of processing, and determines based on the estimation a number of component-processors to operate (abs., lines 1-18; par. [0007]; par. [0017]; par. [0018]; claim 17).

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco and Rawson because Rawson teaching of estimating the workload and determines based on the estimation a number of component- processors to operate would benefit the system performance, improve system resource usage and increase power saving.

31. The combined teaching of Branco, Macias and Rawson does not explicitly teach that a main processor that provides a demand for signal processing to the signal processing device.

32. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching of Branco, Macias and Rawson and especially Branco teaching (col. 3, lines 55-64) that the command to the

controller is generated from an outside source which is a main processor providing a demand for signal processing to the signal processing device as claimed.

33. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537) , in view of Rawson, III (US 2003/0115495 A1) as applied to claim 7 and further in view of Takeda et al. (US 2002/0068626 A1).

34. As per claim 8,the combined teaching of Branco, Macias and Rawson does not explicitly teach a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are determined in accordance with the digital information.

35. However, Takeda teaches a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal

processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are determined in accordance with the digital information (Fig. 1; fig. 2; par. [0033]; par. [0035]; par. [0045]; par. [0046]; par. [0047]; par.[0052]).

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson and Takeda because takeda teaching would elaborate on Branco teaching of command external to the controller which control and generate the demand for signal which is well know to one of ordinary skill in the art to have a master or main processor regulating the demand for the signal and slave processors performing the tasks.

37. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, III (US 2003/0115495 A1) and in view of Takeda et al. (US 2002/0068626 A1) as applied to claim 8 above, further in view of McNeil et al. (US 4,876,643).

38. As per claim 9, Branco teaches that through the management processor, the operating environments is constructed for processing on one or more of the component-processors through the management processor, and, after constructing the operating environments, reconstructs said operating environments to new operating environments upon receipt of another digital information which differs from said digital information

(col. 3, lines 43-67; col. 4, lines 1-16).

39. The combined teaching of Branco, Macias, Rawson and Takeda does not explicitly teach that the constructing and reconstructing is done by the main processor. However, McNeill teaches that the constructing and reconstructing is done by the main processor (col. 3, lines 50-60; col. 4, lines 35-53).

40. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson and McNeil because McNeil teaching would elaborate on Branco teaching of command external to the controller which control and generate the demand for signal which is well know to one of ordinary skill in the art to have a master or main processor regulating the demand for the signal and slave processors performing the tasks.

41. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branco et al. (US 5,630,161) and in view of Macias et al. (US 5,886,537), in view of Rawson, III (US 2003/0115495 A1) and further in view of Takeda et al. (US 2002/0068626 A1) as applied to claim 8 above, and further in view of Gorgone et al. (US 2003/0200249 A1).

42. As per claim 10, the combined teaching of Branco, Macias, Rawson and Takeda does not explicitly teach the digital information comprises plural kinds of application programs that can execute required functions, respectively, and wherein the management

processor assigns any of the functions to the corresponding component-processors, and reads the application program for executing the assigned function from the storage means, and executes the application program.

43. However, Gorgone teaches plural kinds of application programs that can execute required functions, respectively, and wherein the management processor assigns any of the functions to the corresponding component-processors, and reads the application program for executing the assigned function from the storage means, and executes the application program (Par. [0016]).

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Branco, Macias, Rawson , Takeda and Gorgone because Gorgone teaching of processing plurality of application kinds with different function would improve the performance and efficiency and the diversity of processing application and increase the throughput.

45. As per claim 11, McNeill teaches that each of the component-processors operates only for executing the application program for executing the function assigned to the component- processor until the management processor provides another demand to the component-processor (abs., lines 3-9; col. 3, lines 50-60).

Response to Arguments

46. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

48. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

49. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

50. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Caroline Arcos/
Examiner, Art Unit 2195